A Micromachined Tunneling Accelerometer

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6.777 Final Project

Outline of Presentation

- Introduction
- Mechanical Analysis
- Macromodel Simulation
- Electrical Circuit Analysis
- Fabrication Process

Why An Accelerometer?

- Accelerometers have a well established market, mainly 50g devices for airbag modules.
- Accelerometer market is expanding from its base in the automotive industry to industrial and consumer applications.
- Most non-automotive applications require high sensitivity, low g accelerometers.
- The change in requirements represents an opportunity for new accelerometer technology.

Why Tunneling?

- Most accelerometers measure change in capacitance due to displacement of a mass.
- Capacitance goes as the square of displacement.
- Tunneling is exponential with displacement.
- The exponential relationship should allow higher resolution in a smaller structure.
- No other AFM mode could be used to build a compact, high sensitivity accelerometer.

What is Tunneling?

- When two conductors are brought into extreme proximity (~1nm) with an applied bias between them, electrons will ‘tunnel’ across the gap.
- The equation for the resulting current is of the form:

$$I_{tun} = I_o e^{-a\sqrt{f}x}$$

where I_{tun} = tunneling current,

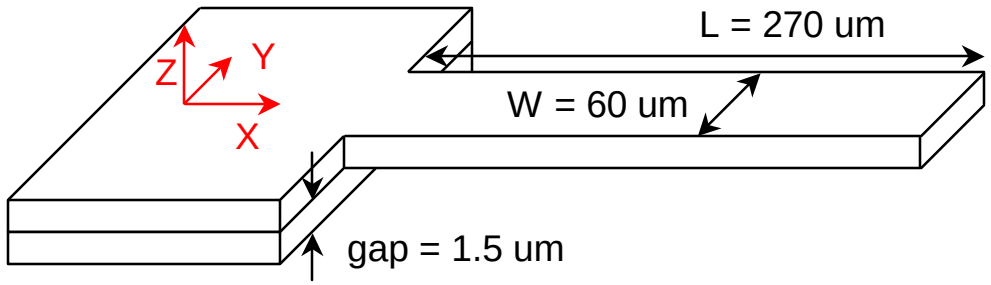
I_o = a constant,

α = tunneling constant,

x = separation and

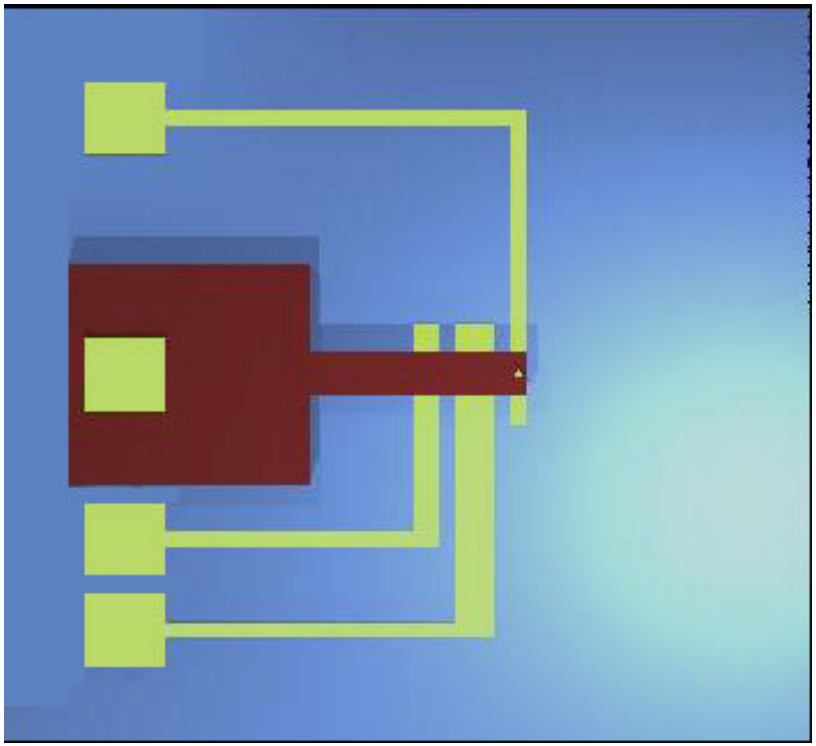
ϕ = tunneling barrier.

Proposed Design



Basic structure is a cantilever with a tip hanging down from the free end. The beam is 2 microns thick with a 1.5 micron gap.

Top View of Proposed Design



1mm square chip.

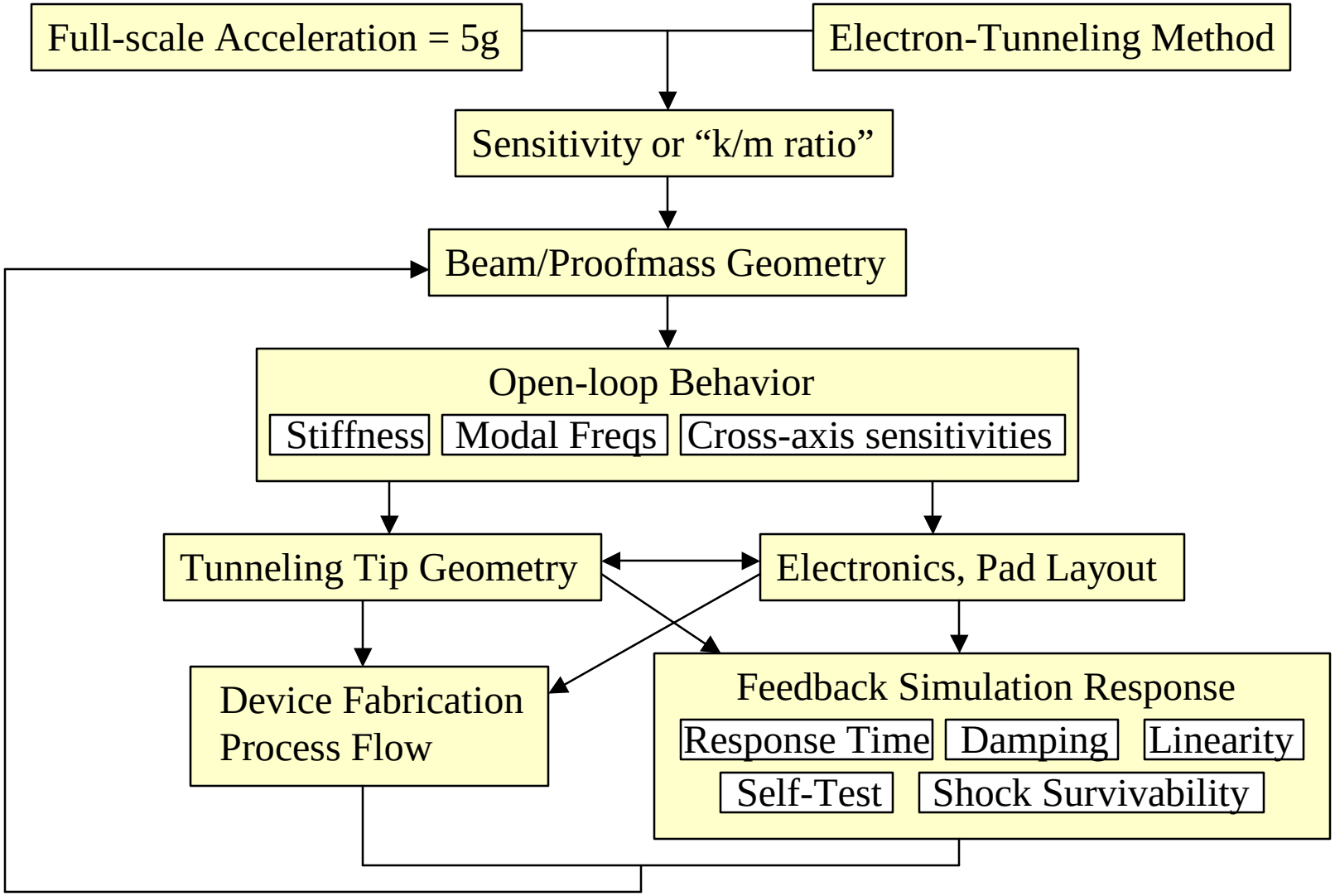
4 connections:

- tip
- sense
- feedback
- self-test

Expected Performance vs Target

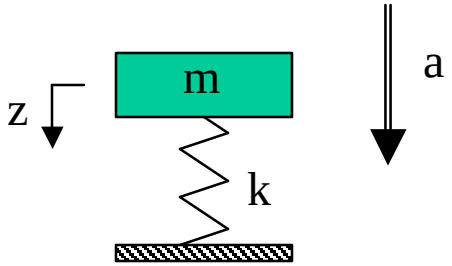
- Design Target
  - 5g range
  - 10ms response time
  - 1% linearity
  - < 1% cross-axis sensitivity
  - 2.5g self test
  - survive 100g powered shock with 1ms rise time
- Simulation Results
  - 20g @ 5kHz
  - 35 μs response time
  - 1% linearity
  - 0.0003 % cross-axis sensitivity
  - 2.5g self test
  - survive 100g powered shock with 1 ms rise time

Design Process Flow



Accelerometer Sensitivity, "k/m ratio"

Static force balance on proofmass: $F_{acceleration} = F_{proofmass/spring}$



$$m\,a = k\,z$$

$$\text{sensitivity} = \frac{z}{a} = \frac{m}{k}$$

Electron-tunneling approach:

- Full-scale acceleration = 5g
- Displacement range ~ 1 Å

sensitivity ~ 2×10^{-12} s^2
"k/m ratio" ~ 5×10^{11} s^{-2}

Other approaches (capacitive, piezoresistive):

- Full-scale acceleration = 5g
- Displacement range ~ 1000 Å

sensitivity ~ 2×10^{-9} s^2
"k/m ratio" ~ 5×10^{8} s^{-2}

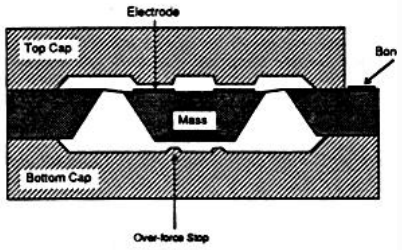
Proofmass Geometry

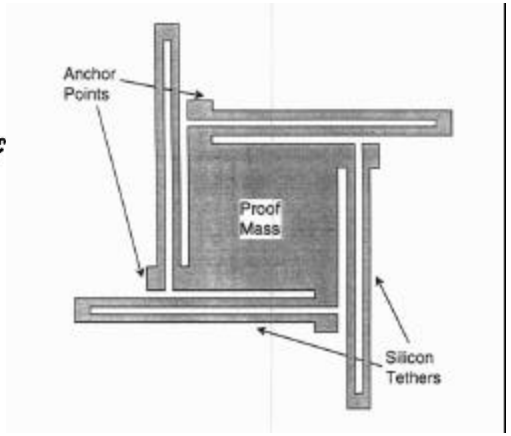
Large sensitivity proofmass:

- Larger mass
- Lower stiffness

} Small k/m

- Bulk micromachined



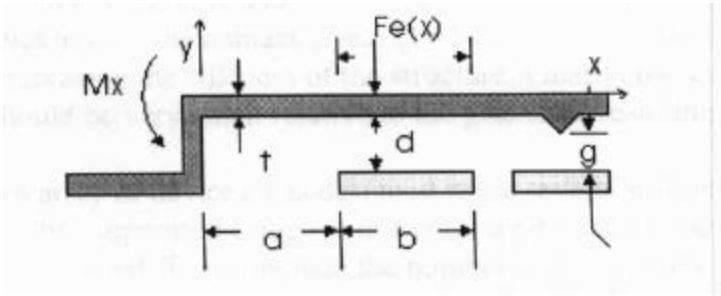


Small sensitivity proofmass:

- Smaller mass
- Higher stiffness

} Large k/m

- Surface micromachined



Advantages in beam geometry:

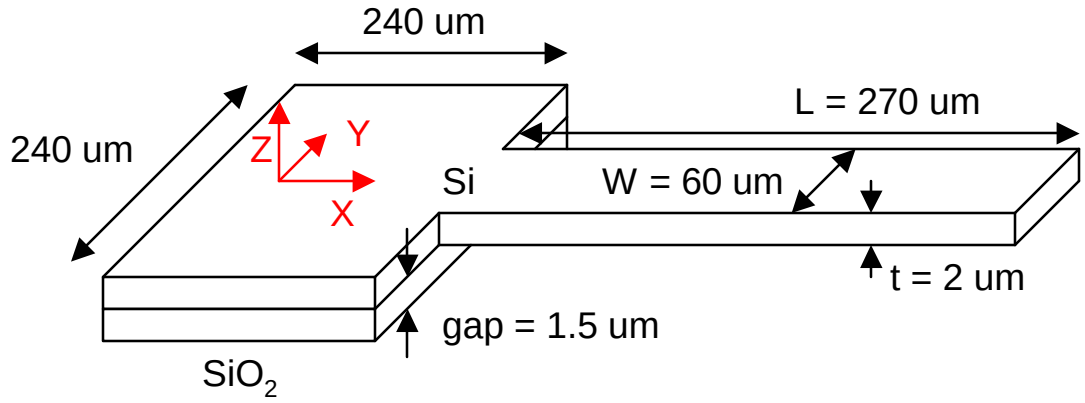
- Reduced cross-axis sensitivity
- Faster response time ($\omega_n^2 \sim k/m$)
- MODELING SIMPLICITY

Electron Tunneling Accelerometer

Final Geometry

Final Geometry:

Tip: 2um x 2um x 1.3 um
(on underside of beam)



Performance Characteristics:

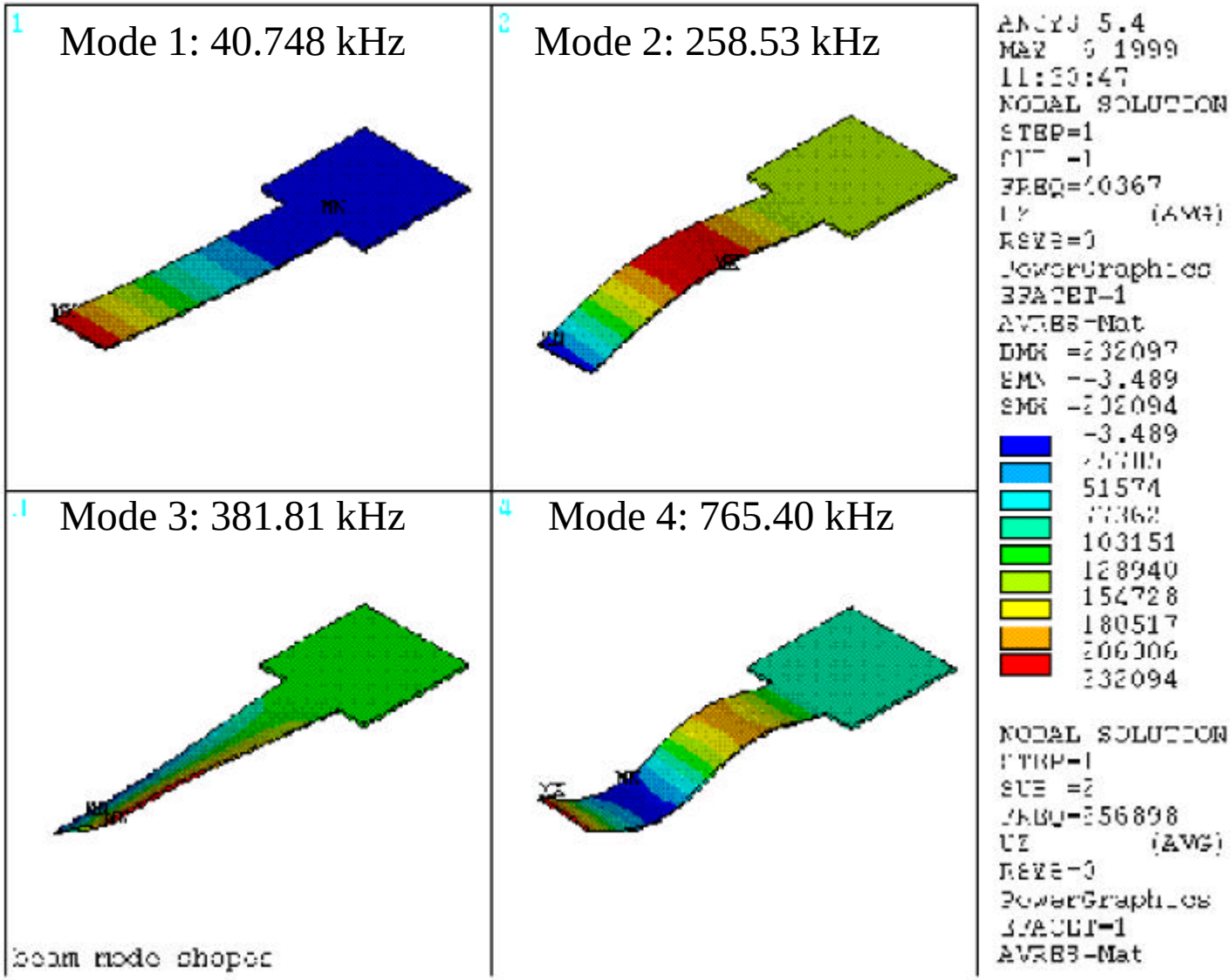
- Open-Loop Z-axis sensitivity = 1.16 x 10^{-11} s^2
- Cross-axis sensitivity ~ 0.0003%
- Modal Frequencies: 40.748 kHz [1st Z-bending]
  258.53 kHz [2nd Z-bending]
  381.81 kHz [1st torsion]
  765.40 kHz [3rd Z-bending]

Issues:

- 1st Beam geometry → holes for SiO2 etching
  Result: underdamped response
  Solution: eliminate holes in beam
  Solution: eliminate holes in beam & increase beam width

Electron Tunneling Accelerometer

Beam Modal Behavior

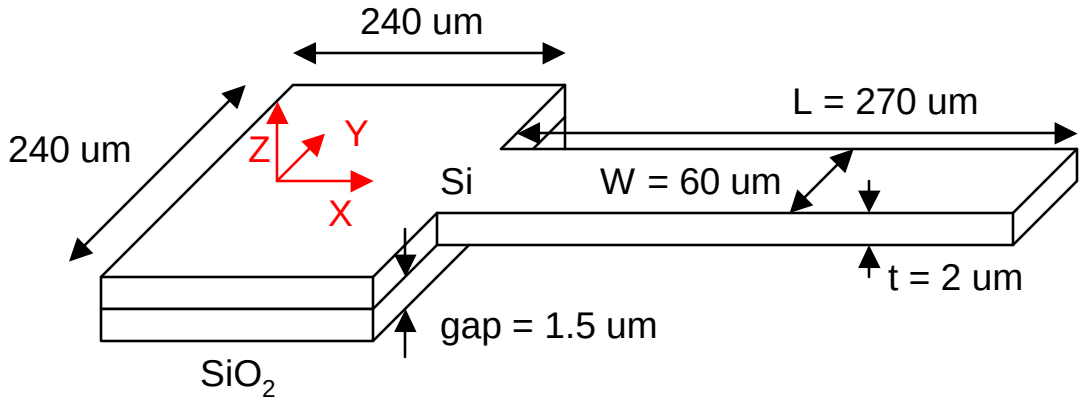


Electron Tunneling Accelerometer

Final Geometry: 5% Tolerance Analysis

Final Geometry:

Tip: 2um x 2um x 1.3 um
(on underside of beam)



± 5% in beam dimensions, properties:

- L, length
- W, width
- t, thickness
- E_{Si}, Young's Modulus
- ρ_{Si}, density

More detailed studies:

- Base dimensions
- Base material
- Varying t (0.95 → 1.05) across width
- Varying t (0.95 → 1.05) along length
- Varying t (1.05 → 0.95) along length
- Presence of tunneling tip
- Offset of tunneling tip

Conclusions:

Cross-axis sensitivity < 1%

$f_{2nd\text{-}mode} > (6.3) f_{1st\text{-}mode}$

Electron Tunneling Accelerometer

Open-Loop Behavior ® Closed-Loop Behavior

Open-Loop Analyses (analytical & finite-element):

- Beam stiffnesses
- Modal frequencies
- Cross-axis sensitivities

Closed-Loop Feedback Analyses (matlab, simulink):

- Closed loop Z-axis sensitivity
- Damping
- Response time
- Linearity
- Self-test
- Shock-survivability

System Model

Cantilever beam

$$m\ddot{z}_t + b\dot{z}_t + kz_t = -y_1(x_t)y_1(x_a)F_a - y_1(x_t)y_1(x_{st})F_{st} - rAy_1(x_t)\int_0^L y_1(x)dx \quad a$$

$$y_i(x) = (\sin(l_i L) + \sinh(l_i L))(\cos(l_i x) - \cosh h(l_i x)) + (\cos(l_i L) + \cosh(l_i L))(\sinh(l_i x) - \sin(l_i x))$$

Squeeze film damping

$$b = \frac{96mLw^3}{p^4 g^3}$$

Electrostatic Forces

$$F_a = \frac{e_o A_a V_a^2}{2\left(g_a + \frac{y_1(x_a)}{y_1(x_t)} z_t\right)^2} \qquad F_{st} = \frac{e_o A_{st} V_{st}^2}{2\left(g_{st} + \frac{y_1(x_{st})}{y_1(x_t)} z_t\right)^2}$$

Feedback Electronics

- Two trans-impedance amplifiers: parasitic capacitance.
- ADC/DAC: Effects of sampling, quantization.

Beam Design: Dynamic Considerations

Preliminary static design:

beam 225 x 30 x 2 μm
bending 58 kHz (Q ≈ 6)
torsion 450 kHz.

Potential fabrication process: holes in cantilever for its release $\Rightarrow$ Q ≈ 48.

Active damping (Q ≈ 0.5) requires high-bandwidth electronics.

- Parasitic capacitance (≈ 1 pF), bandwidth 400 kHz.

Change process, increase beam width w.

- Squeeze film damping ($\propto w^3$).
- Torsional-mode frequency ($\propto w^{-1}$).
- Vacuum vs. Air: Q(10 Torr) ≈ 10 Q(atm).

Final design:

beam 270 x 60 x 2 μm
bending 40 kHz (Q ≈ 1)
torsion 381 kHz.

Accelerometer Design

Tunneling current set-point: 2.8 nA (~ 8.5 Å separation).

- Sensitivity.
- Tip crash.

Electrostatic pads

- No pull-in effect: 1.5 mm gap, 1.3 mm tip.
- Location: maximum voltage, fringing effects.

Amplifiers

- Logarithmic amplifier is not used.
- Gain-bandwidth product, 1MHz.

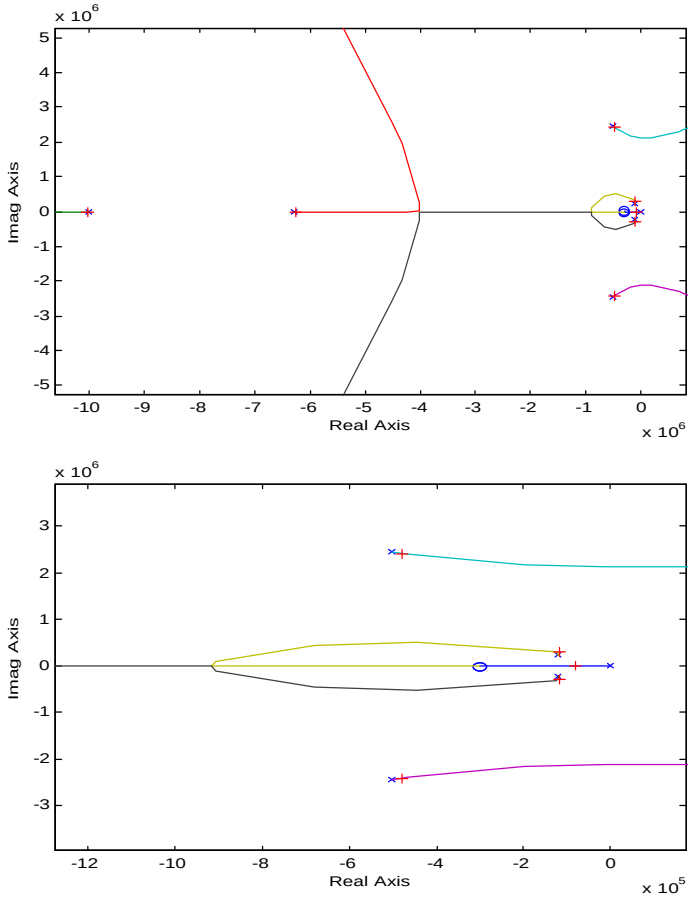
Controller Design

Requirements

- High bandwidth.
- Robust to gain uncertainties (high gain margin).
  - $I_{tun} \approx \begin{cases} 12\,\Delta x & @8.5\,\mathrm{A^o} \\ 52\,\Delta x & @5.0\,\mathrm{A^o} \end{cases}$
- Low sensitivity to amplifiers drift and offset voltages.
- Damping, small settling time, small amplitudes during transients.

PID controller

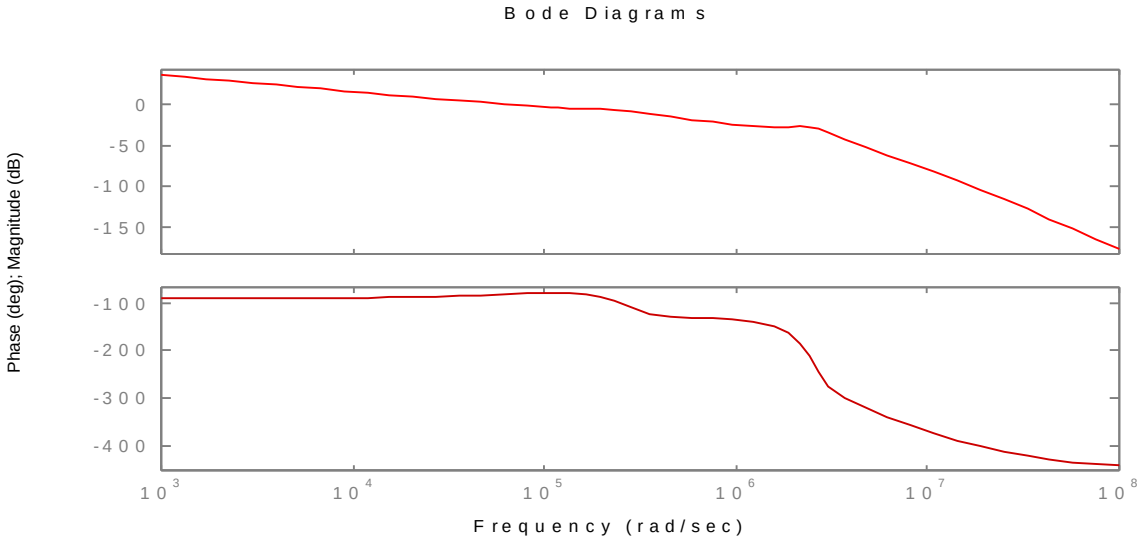
- Additional high-frequency pole.
- Integrator anti-wind-up.



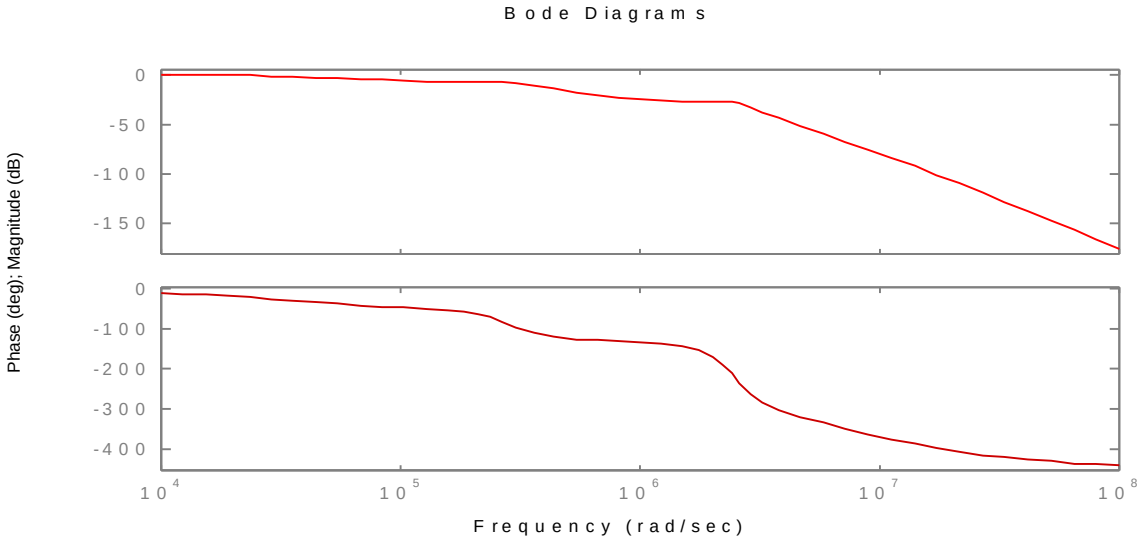
Open/Closed-Loop Frequency Response

Open-loop Frequency Response

- Gain margin ≈ 8.
- Phase margin ≈ 92°.
- Crossover ≈ 9kHz.

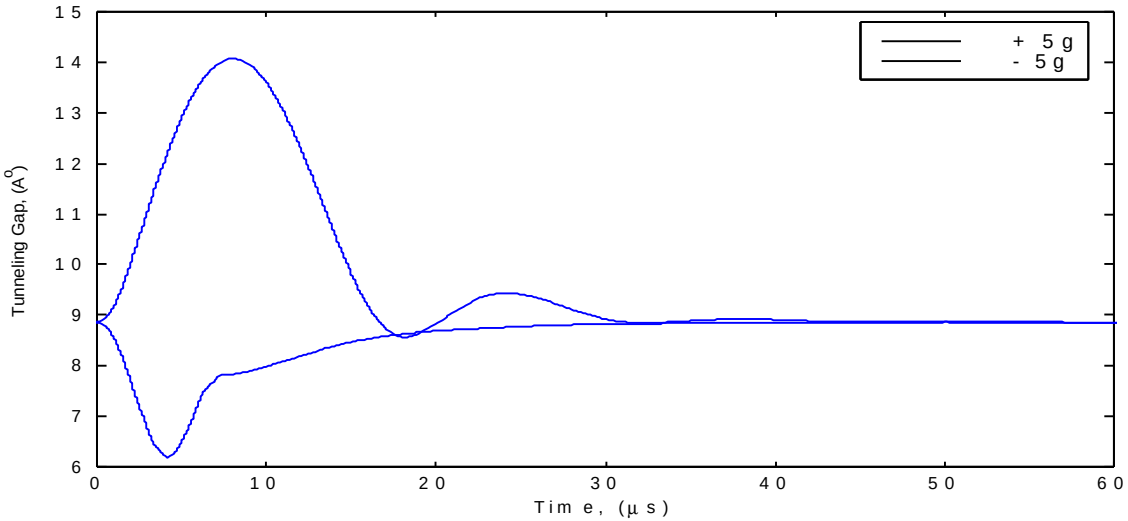


Closed-loop Frequency Response

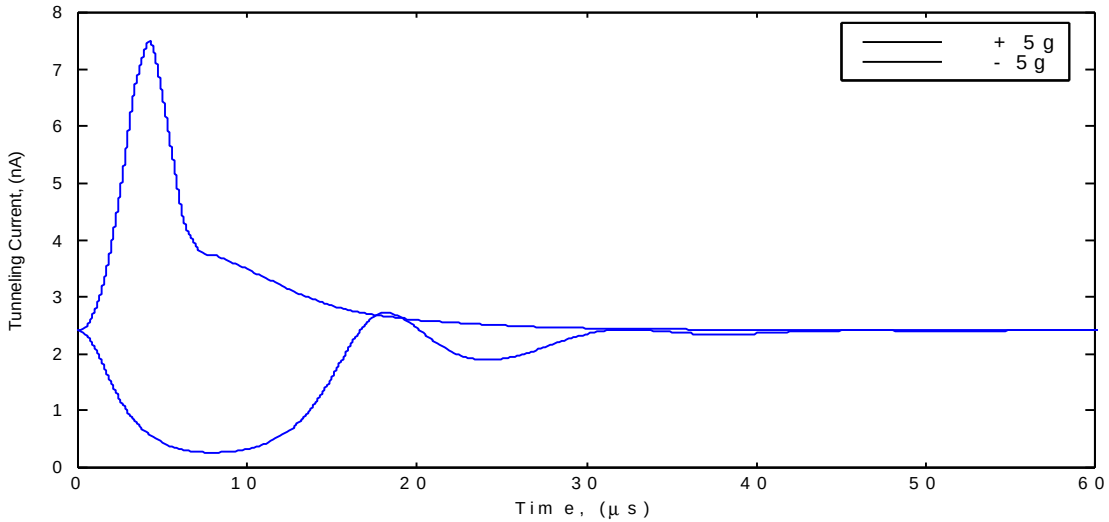


Closed-Loop Step Response: 5g

Tunneling Gap (A^o)

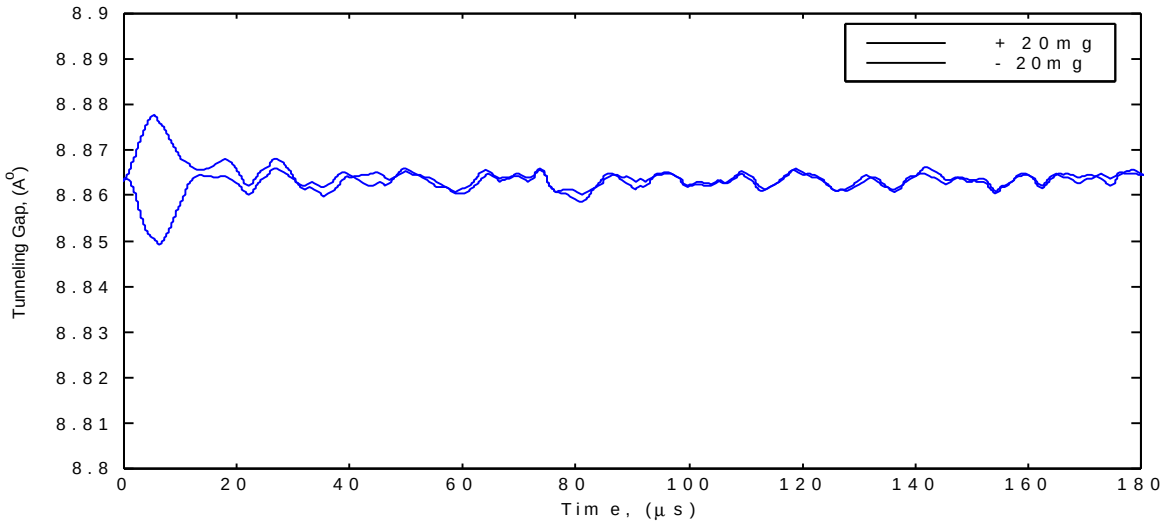


Tunneling Current (nA)

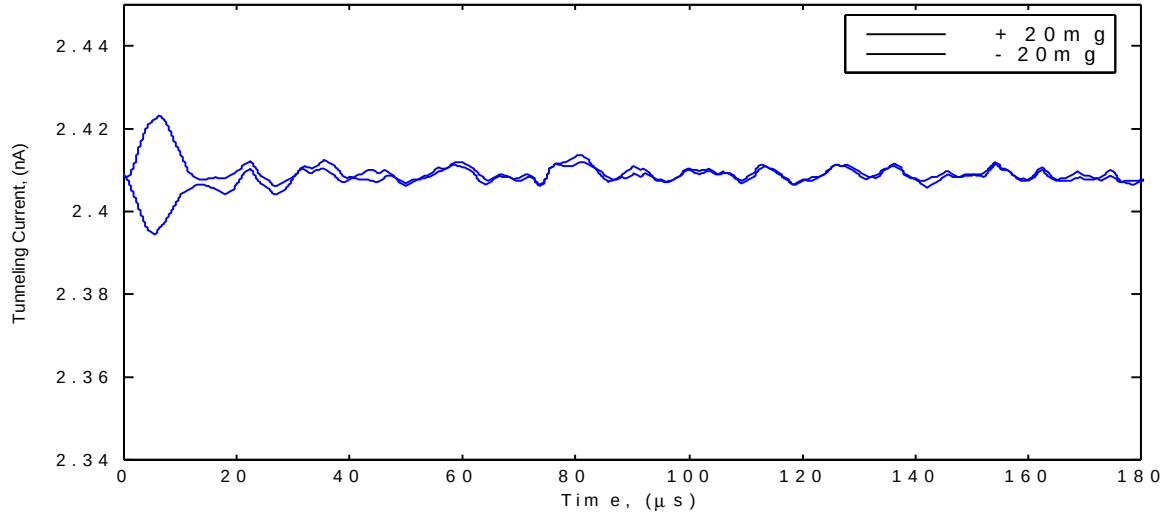


Closed-Loop Step Response: 20mg

Tunneling Gap (A^o)

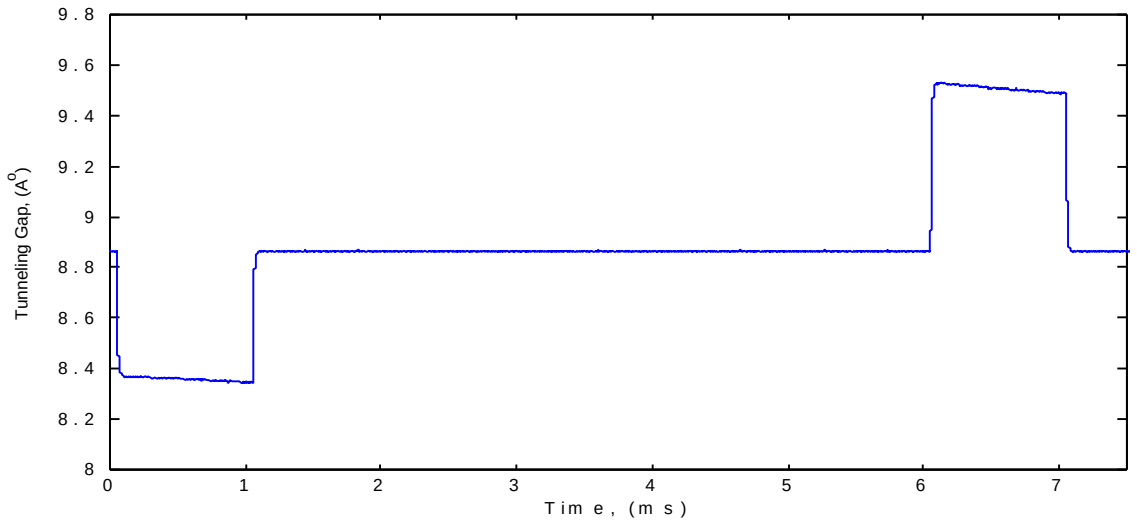


Tunneling Current (nA)

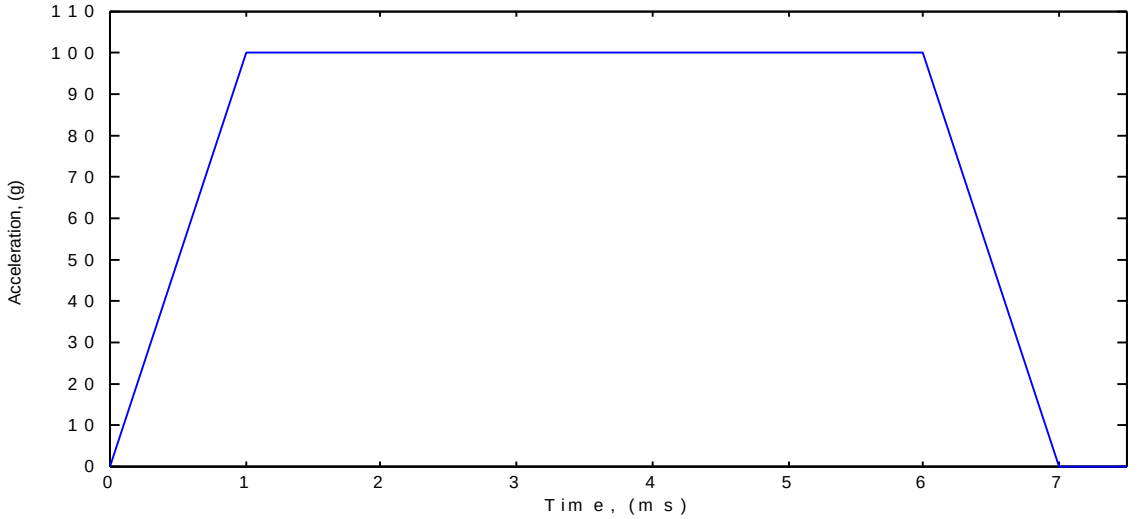


Shock-Test: 100g for 5ms, with 1 ms rise time

Tunneling Gap (A^o)



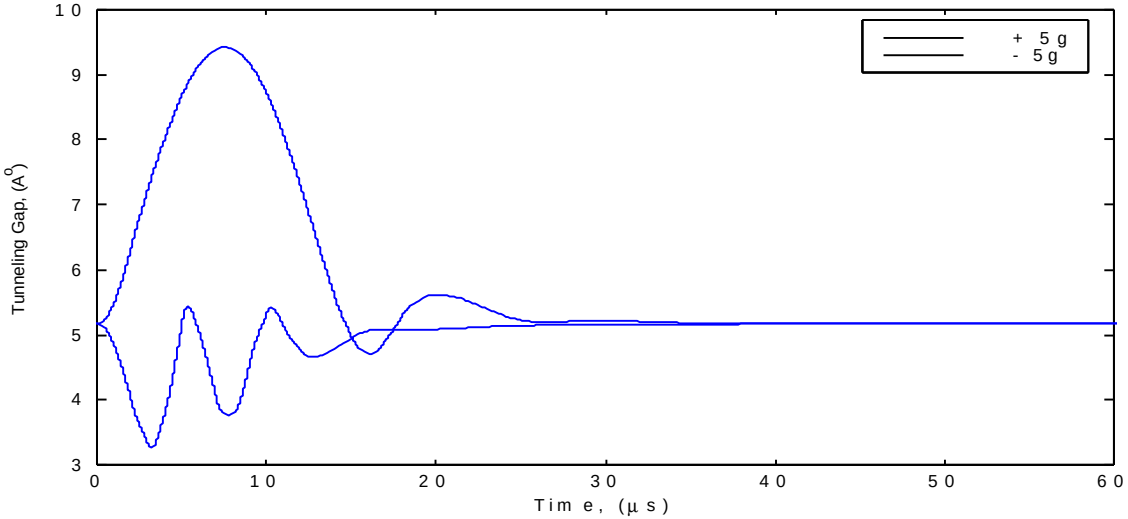
Acceleration (g)



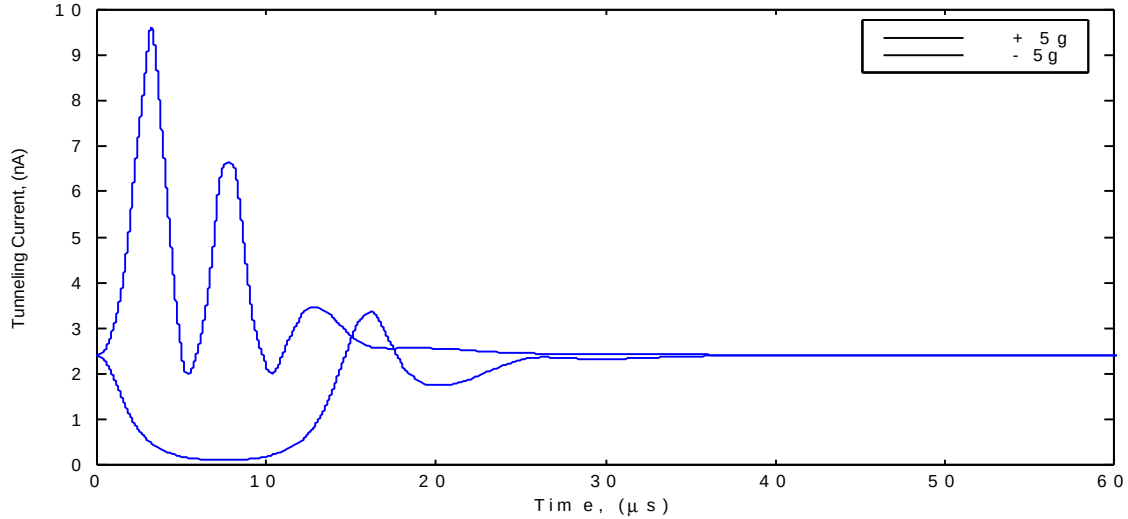
Effect of Parameters: Barrier Height, f_o = 0.17 eV

ϕ = 0.5 eV

Tunneling Gap (Aº)



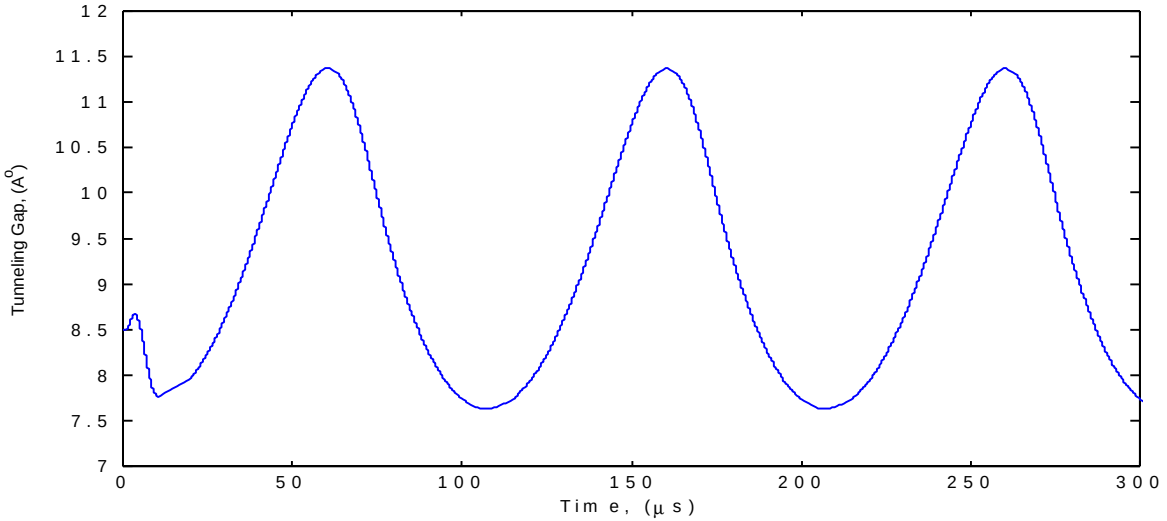
Tunneling Current (nA)



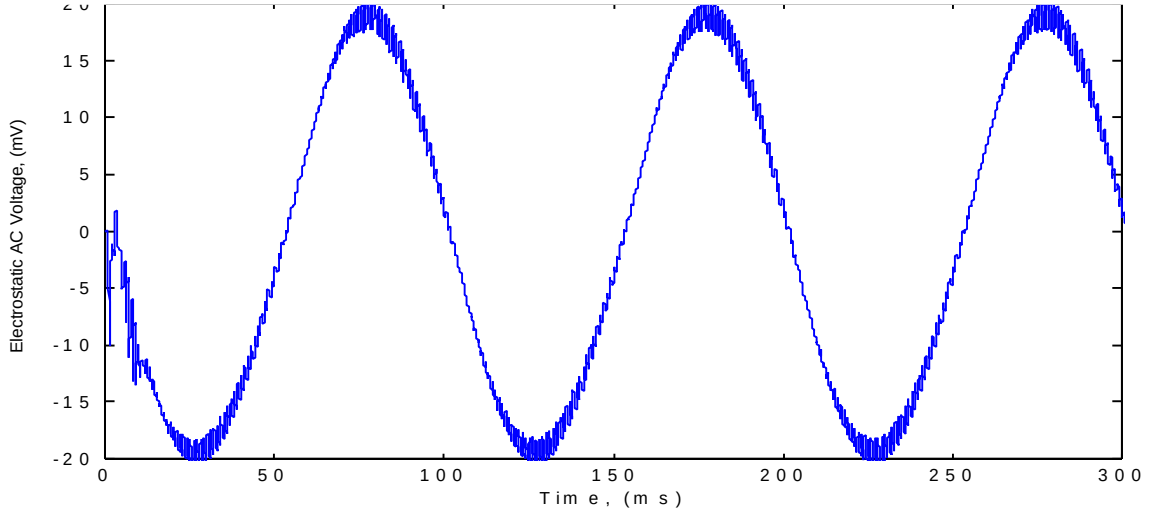
Frequency Response: Nonlinear Simulation

5g 10 kHz

Tunneling Gap (Aº)



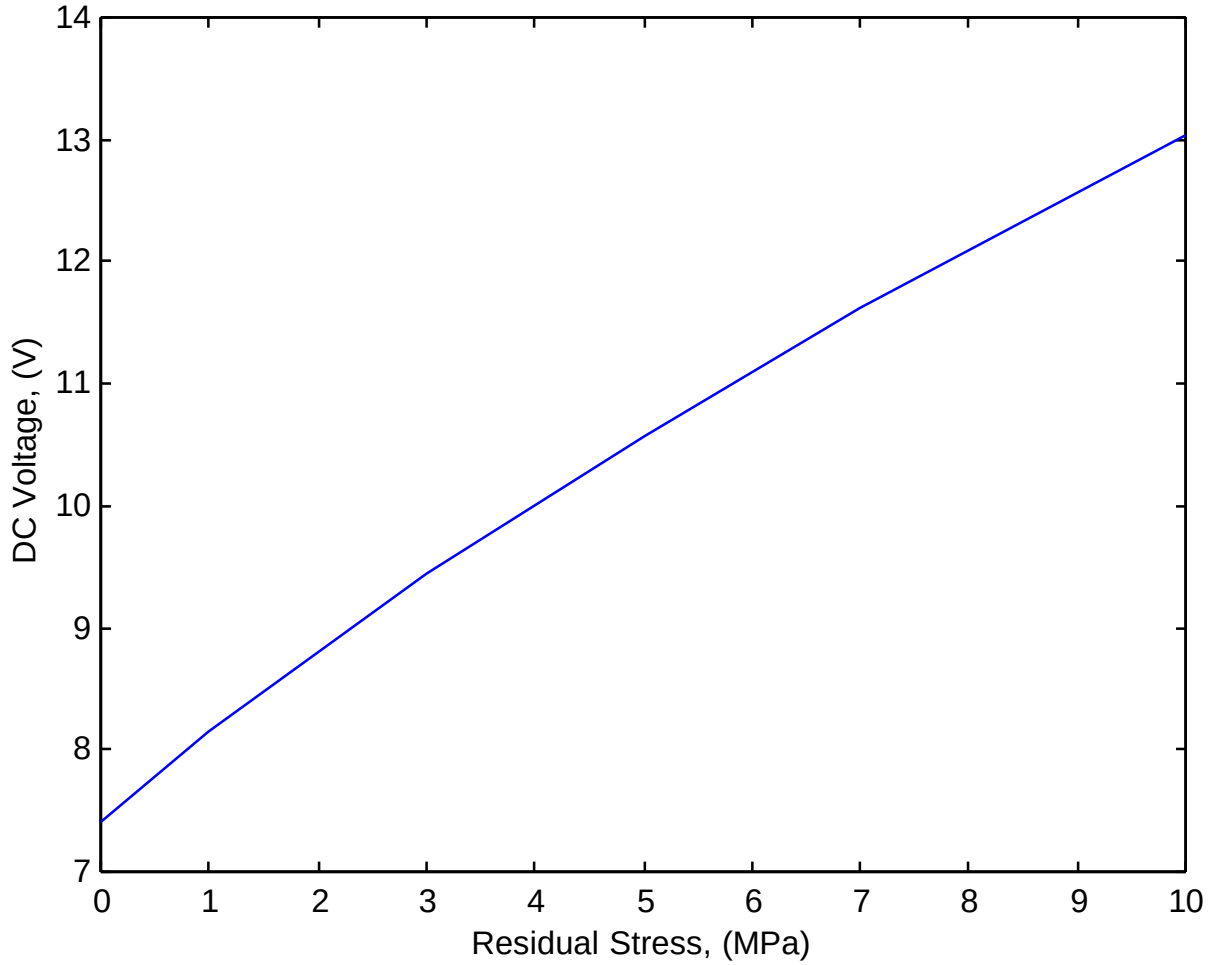
Actuation Voltage (mV)



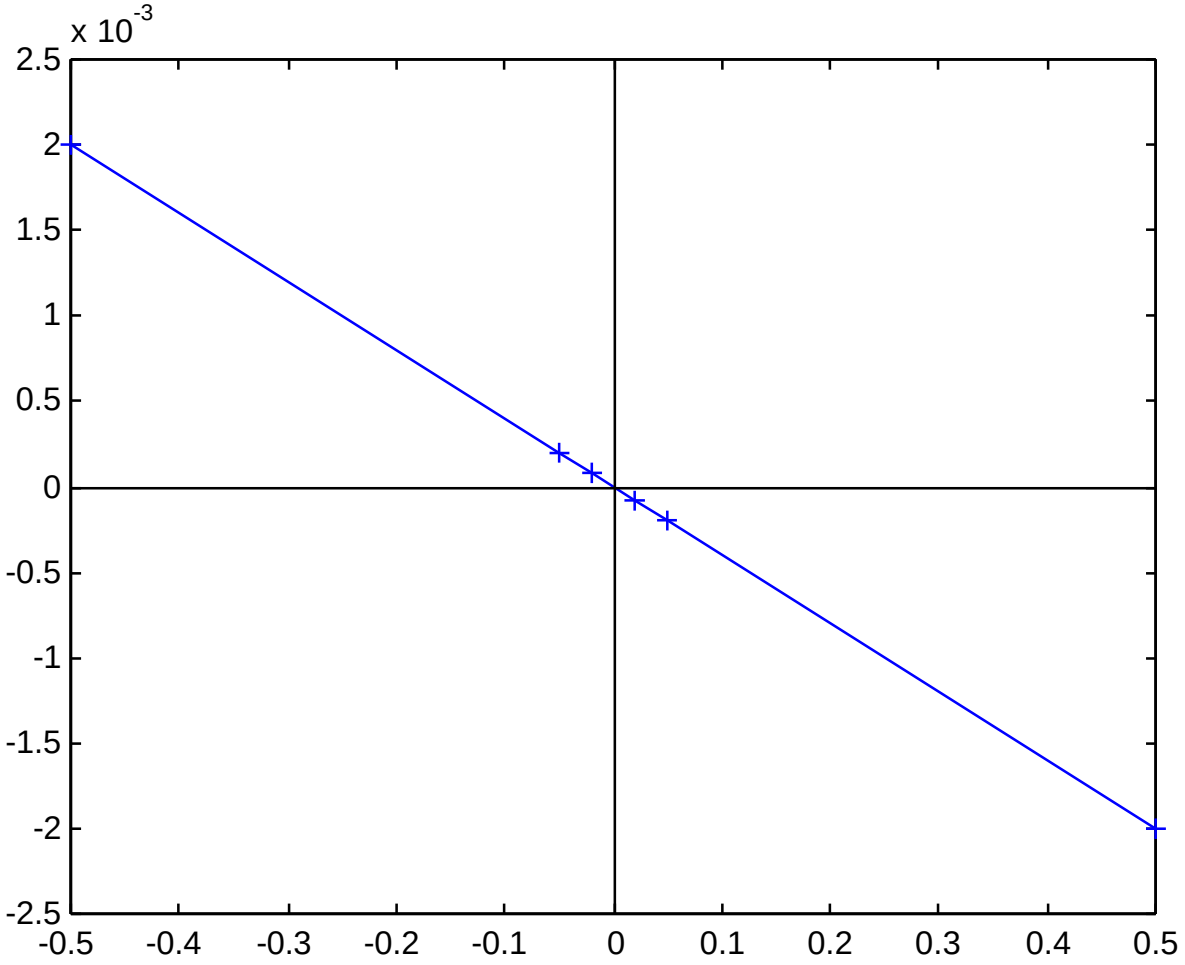
Performance Specifications

Characteristic	Spec	Actual
Full-scale Acceleration	5g	5g (up to 10 kHz) 20g (up to 5 kHz)
Resolution	1 %	0.4 %
Linearity	< 1 %	<<1 %
Response Time	< 10 ms	35 us
Self-Test	2.5g	**P**
Cross-axis Sensitivity	< 1 % at 5g	0.0003 % at 5g
Shock Survivability	100g 100ms pulse with 1ms rise time	**P**

Residual Stress



Linearity



Electrical motivations

- One-conductor design: well-decoupled system
  - carries both actuation currents and tunneling current
  - advantage: one fewer mask step
  - tunneling capacitance (2 μm diameter round tip) << control actuator capacitance

$$C_{tunnel} = .26\,fF << C_{actuator} = 11\,fF$$

  - tunneling resistance high compared to power supply output resistance

$$R_{power} \sim 1\Omega << R_{tun} = \frac{0.2V}{1nA} = 200M\Omega$$

  - net result - capacitive actuator doesn't affect tunneling

$$I = C_{ac}\frac{dV_{ac}}{dt} = (10.6\,fF)\frac{13mV}{.15ms} = 0.92\,pA << I_{tun} \sim 1nA$$

- Three pads with different scales of voltages - switching power supplies
  - self-test - 0.7 V across gap causes 2.5 g's: set once with 8-bit DAC
  - control - 10V $\pm$ 15mV across gap: small part controlled with high-speed 14-bit DAC, large part set once with 8-bit DAC
    - may need step-up via charge pump, due to residual stress (~100 V)
  - tunneling-pad - 0.2 V across gap (linearly divided Zener diode)
- Digital, since so many delicate parameters - and may need retuning

Electrical micromodel

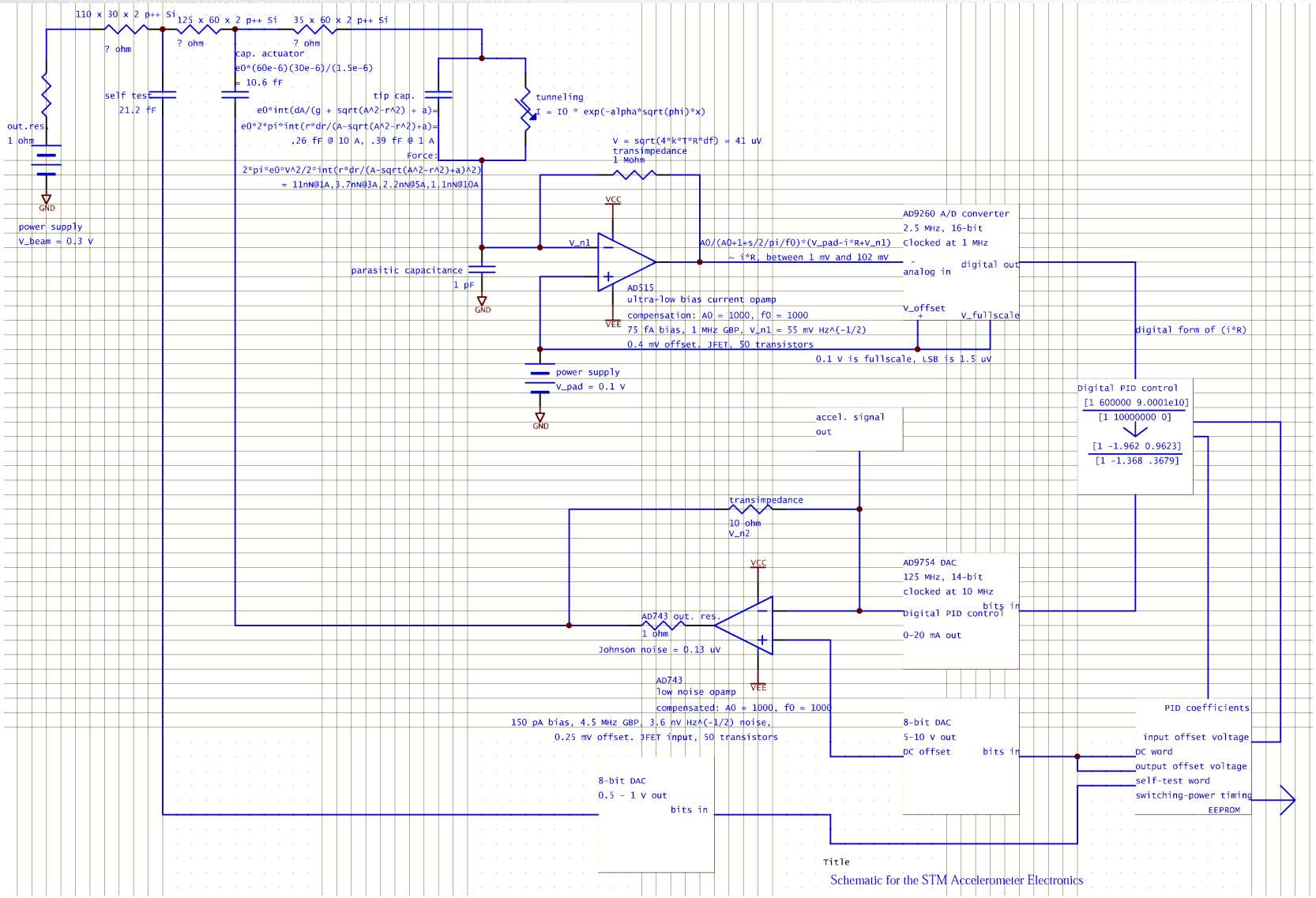
Principles

- Real devices - finite bandwidth, noise, fabrication, size, cost
- Take models from existant parts:
  - technology exists, but represents decades of work
  - specifications reflect behavior of devices of similar functionality

Choices

- Transimpedance input: 75 fA input bias current, 1 MHz GBP, 55 nV $Hz^{-1/2}$ noise 10 Hz-1kHz, 0.4 mV offset - use AD515 macromodel
- DAC: there exists a 125 MHz 14-bit DAC, the AD9754 (50 pA $Hz^{-1/2}$ noise)
- ADC: there exists a 2.5 MHz 16-bit DAC, the AD9260 (30.5 uV $Hz^{-1/2}$ noise)
- Transimpedance output: 3.5 nV $Hz^{-1/2}$ noise 10 Hz-1 kHz - use AD743 macromodel

Main circuit schematic



Evaluation

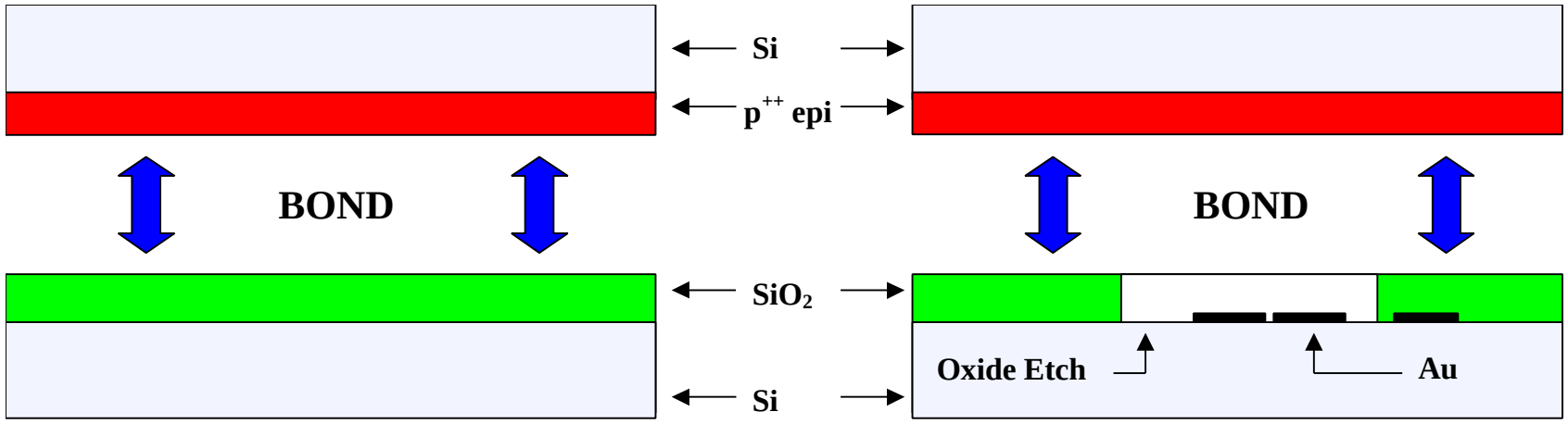
- Size and complexity:
  - each op-amp has roughly 50 transistors - 40 mil x 40 mil
  - DAC: roughly 30 resistors, 15 transistors for current sources, 30 transistors for switching, plus overhead. One good DAC, two cheap DACs. 40 mil x 40 mil
  - ADC: roughly 50 resistors, several hundred transistors for flash, successive approximation (DAC/feedback circuitry), and digital outputs. 50 mil x 50 mil
  - digital control: one adder, one fixed-point multiplier, 400 gates or so
    - synthesize digital logic in Verilog: get ~ 520 gates. 5 mil x 5 mil
- Thus this is all very cheap and can fit on a die that fits in a 2.6 x 2.6 mm^2 square.

Fabrication Based on Modified SOI Process

Fabrication Challenges:

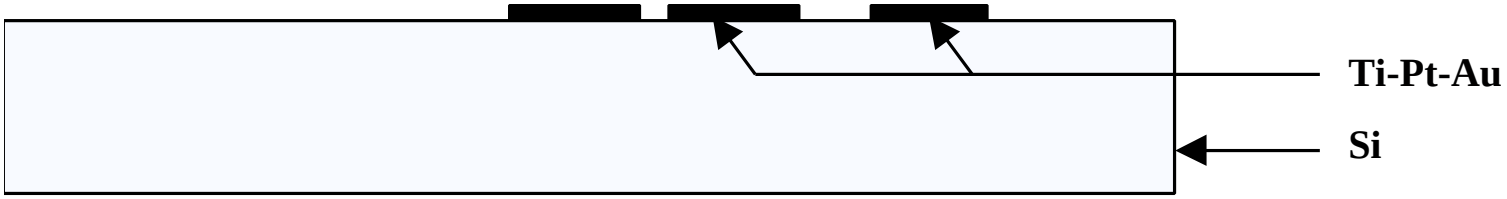
- **Form tip & proof mass from the same wafer**
- **Release cantilever without using etch release holes**

Traditional SOI Wafer Assembly **Modified SOI Wafer Assembly**

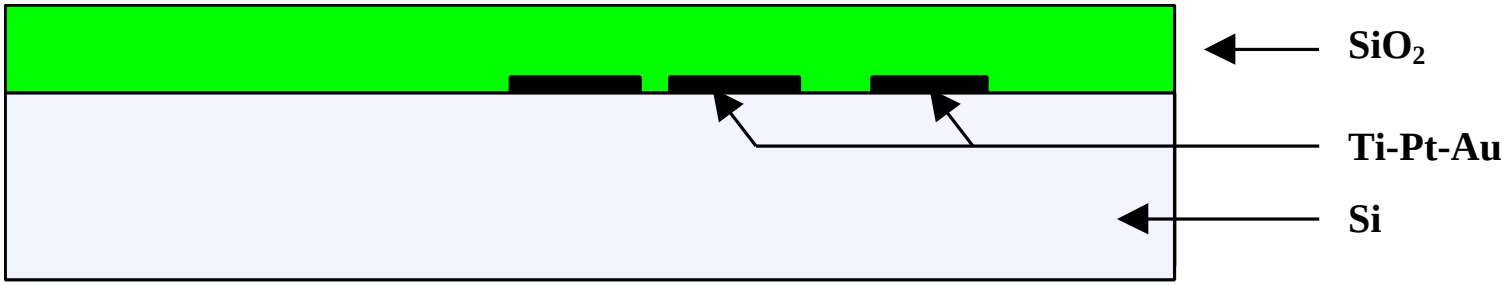


Process Flow

Step 1: Mask #1 --- Metal Pads

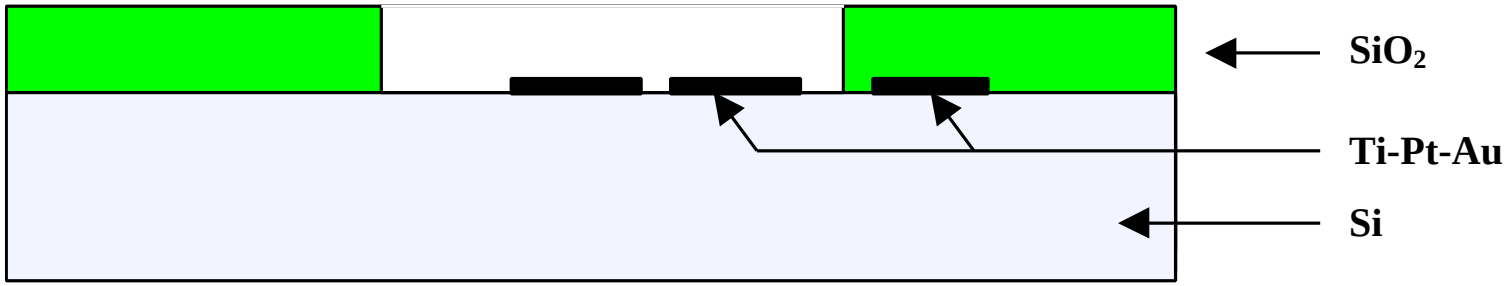


Step 2: Deposit Oxide

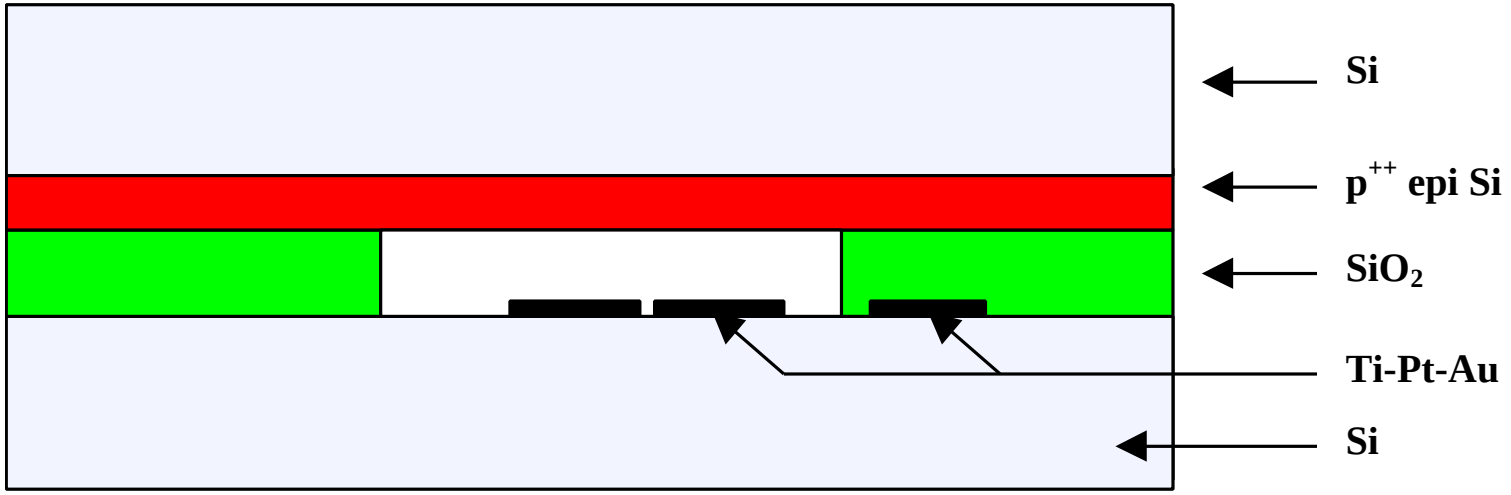


Process Flow (con't)

Step 3: Mask #2 --- Oxide Cavity

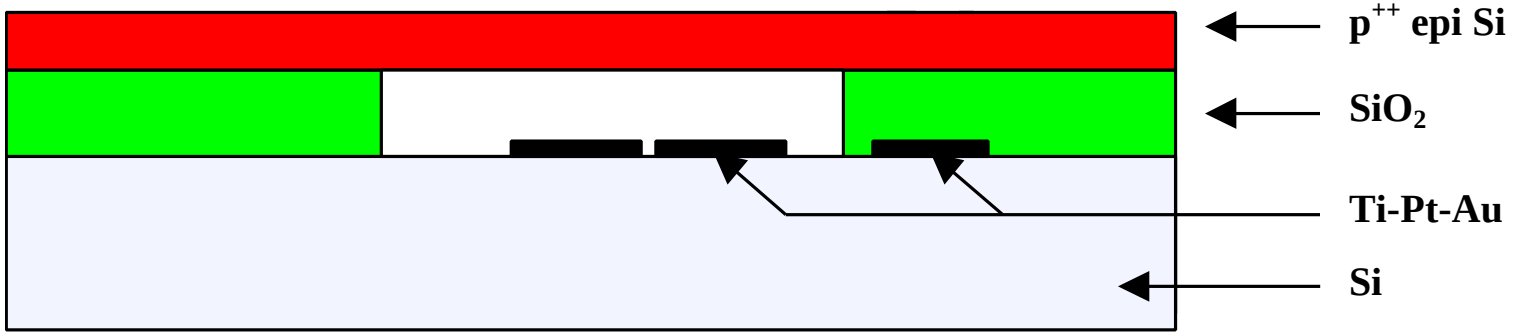


Step 4: Planarize and Bond

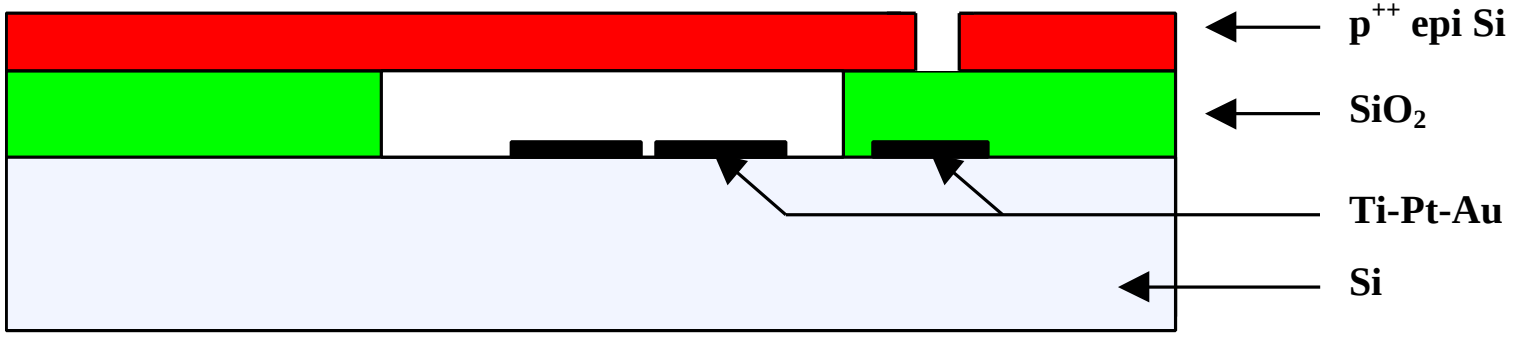


Process Flow (con't)

Step 5: Thin Down to Highly Doped Etch-Stop

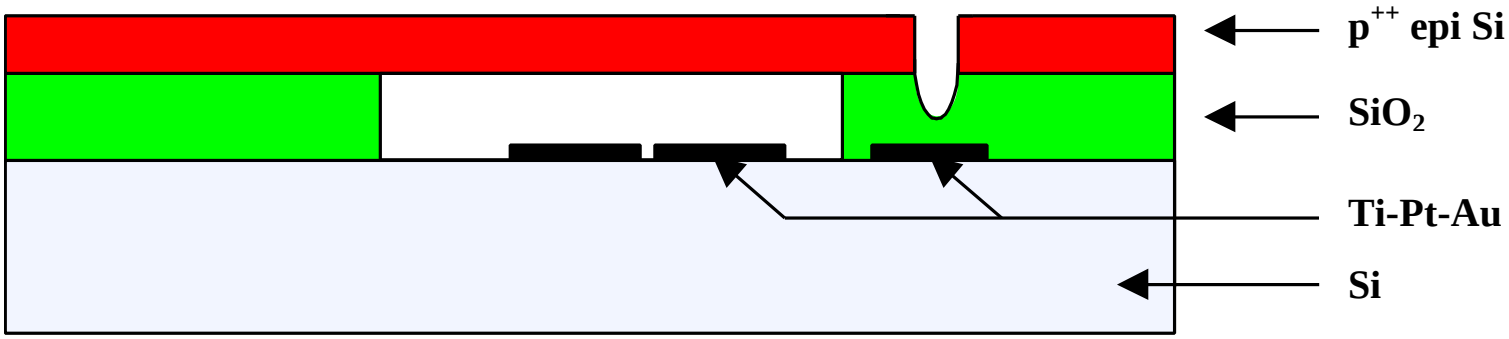


Step 6: Mask #3 --- Etch Tip Hole Through Cantilever Layer

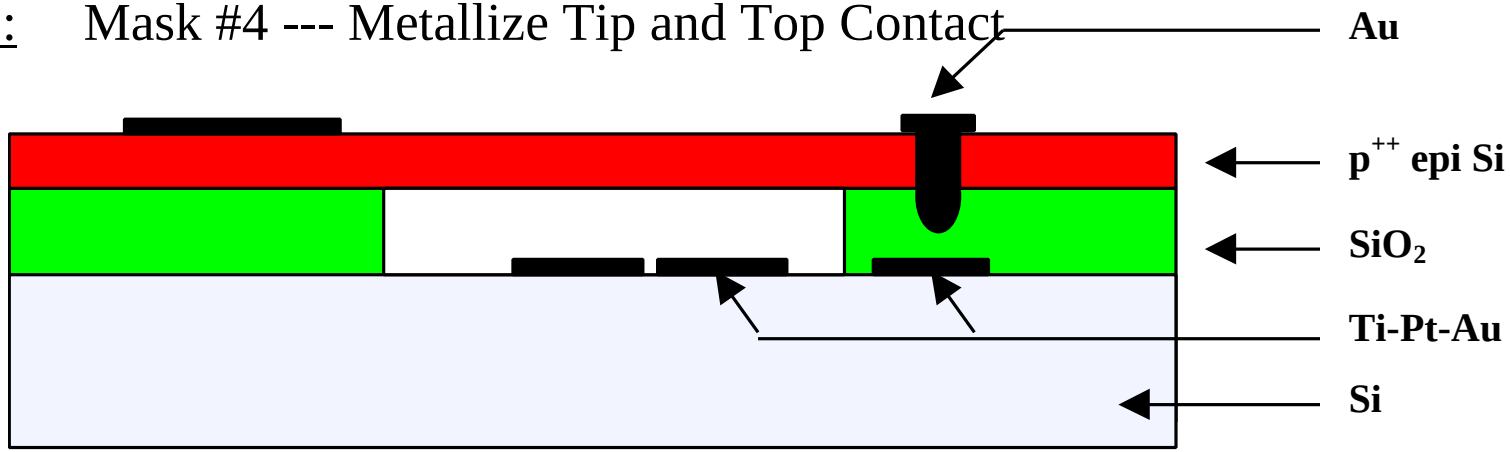


Process Flow (con't)

Step 7: Timed Etch into Oxide to Form Mold for Tip

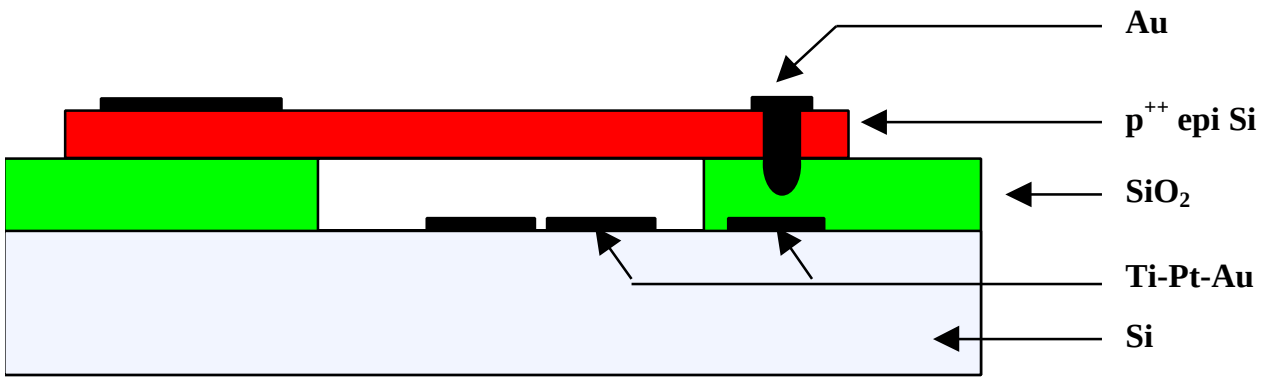


Step 8: Mask #4 --- Metallize Tip and Top Contact

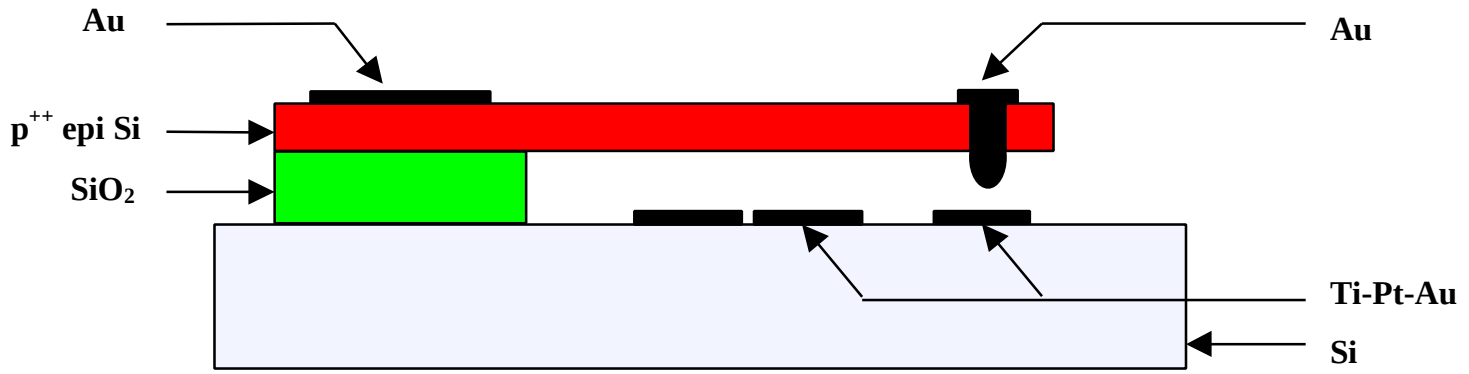


Process Flow (con't)

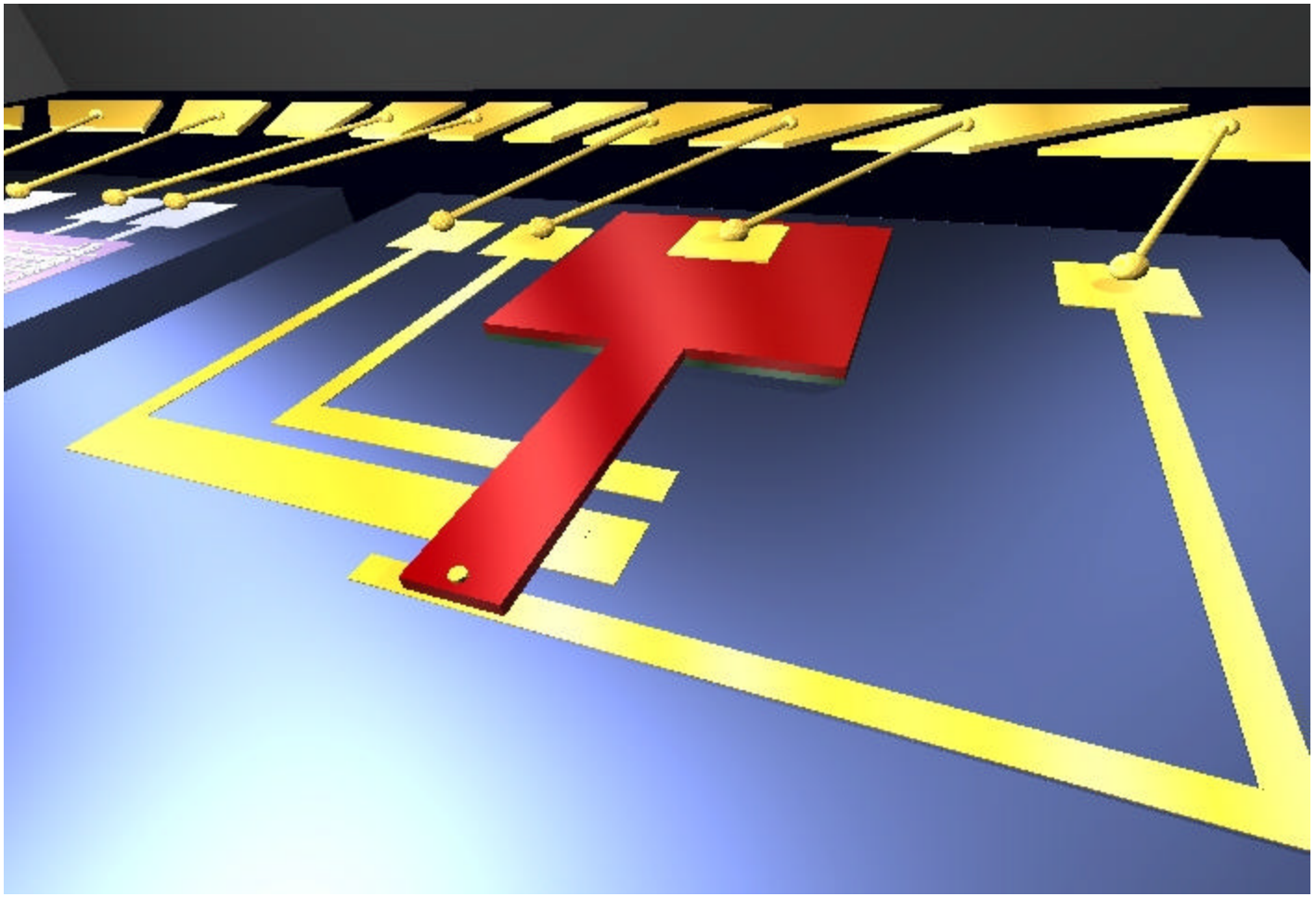
Step 9: Mask #5 --- Define Cantilever



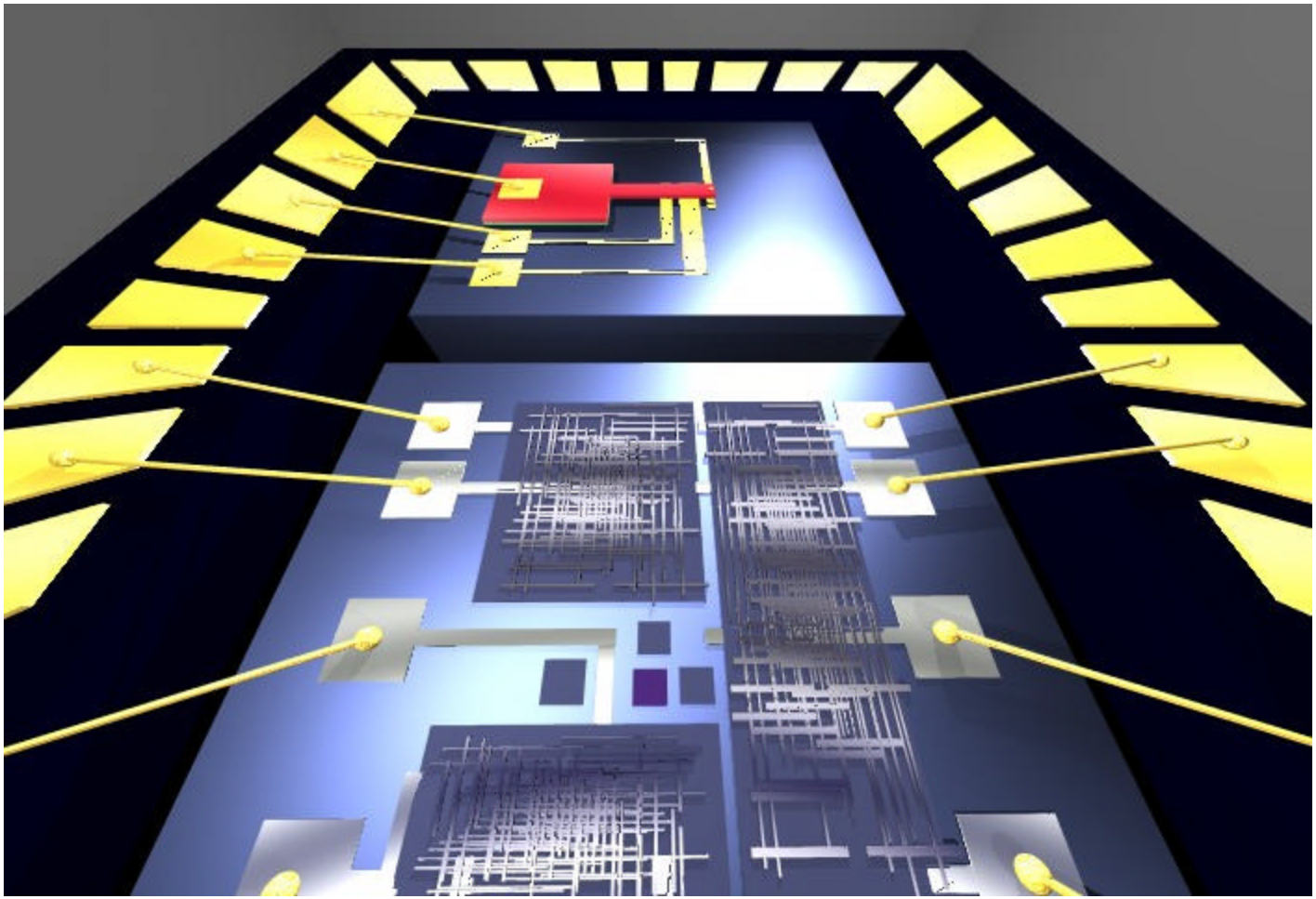
Step 10: Oxide Etch and Release



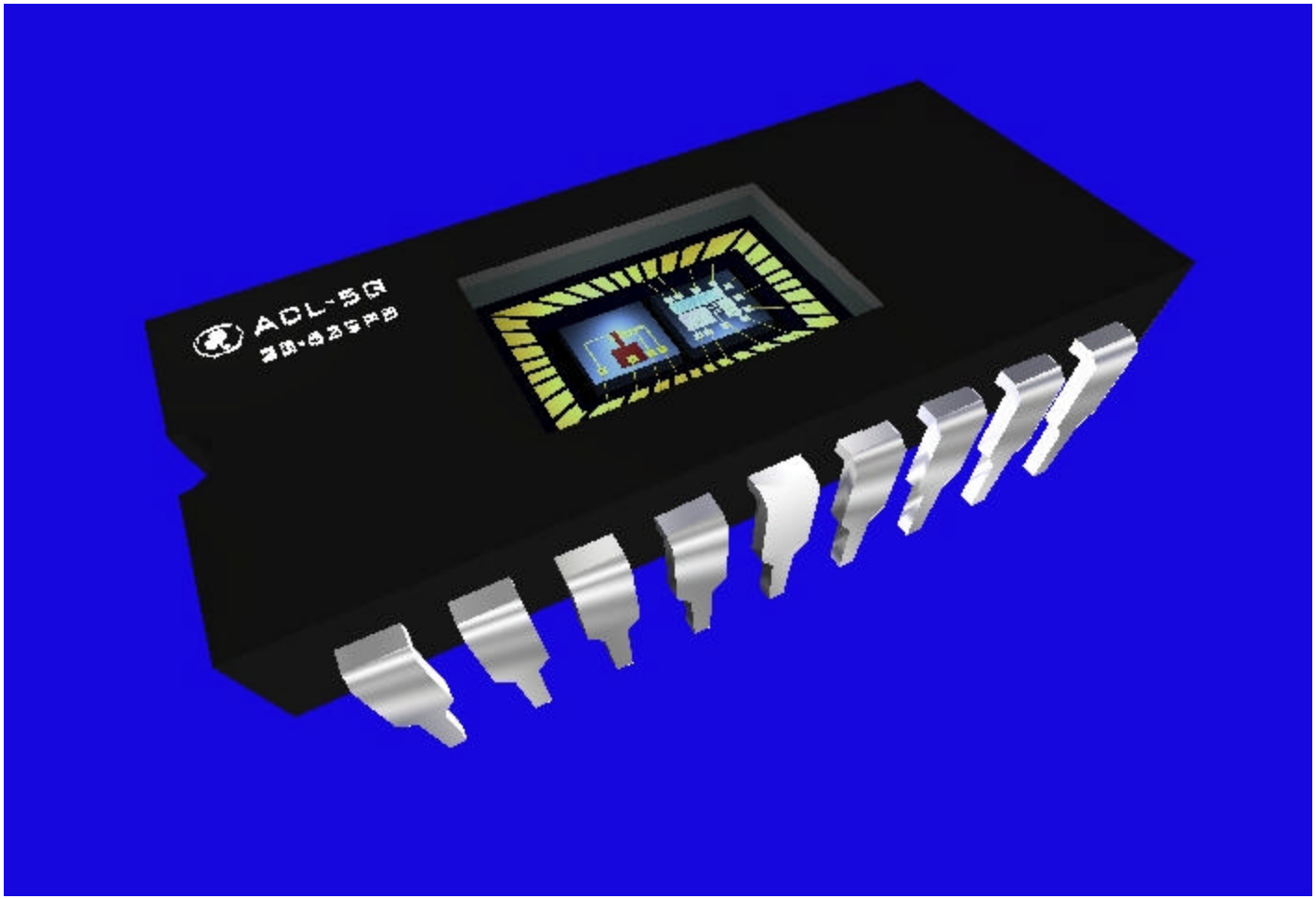
Microcantilever with tunneling tip



Two-chip package



The ACL-5G (third quarter 2002)



Conclusion

- Specification
  - 5g up to 100 Hz
  - 10ms response time
  - 1% linearity
  - 1% cross-axis sensitivity
  - 2.5g self test
  - survive 100g shock with 1ms rise time
- Performance
  - 5g up to 10 kHz
  - 35 μs response time
  - << 1% linearity
  - << 1% cross-axis sensitivity
  - capable of 2.5g self test
  - survive 100g shock with << 1 ms rise time

Additional Considerations

•Residiual Stress - in theory, should be zero

- few fabrication/packaging processes and geometries can even claim zero *theoretical* residual stress, like the cantilever does
- if there is consistent residual stress, we can prestress the beam by adding an appropriate layer to cancel the inherent stress

•Contamination

- using Au as fundamental conducting material. No oxidation problems.
- can work in an N_2 ambient, for improved decomposition sensitivity.
- operation in air over 18 mos. proven with nominal degradation of performance (T. W. Kenny, et. al., JPL/Caltech, "Wide bandwidth…")

Precision Tip Geometry

- Alternate process flow generates a tip with precise geometry and 100 nm tip radius

•Brownian motion of air

- electronic noise dominates (Yeh C., Najafi, K., J. MEMS., 7.1: 3/98)

Additional Considerations (con't)

- Justification for the Cantilever Design vs. Other Geometries
  - no theoretical residual stress due to packaging
  - nature of tunneling signal suggests the need for low mechanical sensitivity (small proof mass)
  - for a given stiffness, a cantilever has smallest size for any canonical geometry
    - can deflect more per unit voltage, allowing greater dynamical range and less stringent fabrication tolerances
  - can pack many devices onto a wafer, giving lower per-die cost
- Vertical Motion Design was Chosen Over Horizontal Motion Design
  - Effective thickness of flexure is more accurately fabricated (10 nm vs. 180 nm)
  - Simple geometry with small footprint